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EXAMINER	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/517,673
Filing Date: July 11, 2005
Appellant(s): MUTH, MATTHIAS

Michael J. Ure
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed on 7/15/08 appealing from the Office action mailed on 1/2/08.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6470393	Heinrich	10-2002
5892893	Hanf I	4-1999

6438462	Hanf II	8-2002

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 22-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heinrich et al (US Patent 6470393), in view of Hanf et al (US Patent 5892893).

For claim 22, Heinrich et al teach the following limitations:

A method of activating an application controller unit (MC in Fig 2) that is coupled to a Controller Area Network bus (lines 10-15 of column 5) and that carries out an application (microcontroller carries out application), comprising:

- a transceiver unit (IF in Fig 2 comprises a transceiver unit as it can transmit or receive the information; lines 10-12 of column 1) receiving an incoming message occurring on the data bus ("activating address" mentioned in lines 61-62 of column 2);

- and the transceiver unit causing a protocol controller unit (address filter "AF" and "ASR" shown in Figure 3) coupled to the application controller unit to be supplied with voltage first, before the application controller unit is supplied with voltage (lines 45-65 of column 2 mention that activating demand on bus causes activating address filtering. Thus, address filter is supplied with voltage first. When intended address is received, the microcontroller is supplied with the voltage);

- wherein the protocol controller unit is provided with a crystal oscillator input signal (lines 36-67 of column 10 mention that a quartz oscillator is provided in the system for synchronization. The clock master with quartz oscillator reacts emission of a predetermined clock definition bit sequence. Fig 3 shows that ASR receives bit sequences Rx. Thus, quartz oscillator input is provided to the protocol controller).

Heinrich does not teach that the transceiver and protocol controller are provided on different integrated circuits. Hanf et al teach a system where transceiver (100 in Fig 1) and protocol controller (22 in Fig 1) are provided on different integrated circuit.

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Heinrich and Hanf. One ordinary skill would be motivated to put the transceiver unit in different integrated circuit, as that would lead to a

more flexible and modular design. Any commercially available transceiver chip may be used with the existing system.

For claim 23, address filter stores the reference message and compared with the incoming message stored in ASR that is provided by transceiver unit. If they are same transceiver releases a connection for microcontroller (lines 20-60 of column 5 of Heinrich).

For claim 24, note lines 60-65 of column 2 of Heinrich.

For claim 25, Heinrich et al teach the following limitations: A system comprising for use with a Controller Area Network data bus (Fig 1; lines 10-15 of column 5), the system comprising:

- an integrated circuit comprising a transceiver unit coupled to the data bus (IF in Fig 2 comprises a transceiver unit as it can transmit or receive the information; lines 10-12 of column 1);
- and a protocol controller unit (address filter “AF” and “ASR” shown in Figure 3) having a crystal oscillator input signal (lines 36-67 of column 10 mention that a quartz oscillator is provided in the system for synchronization. The clock master

with quartz oscillator reacts emission of a predetermined clock definition bit sequence. Fig 3 shows that ASR receives bit sequences Rx. Thus, quartz oscillator input is provided to the protocol controller) and coupled to the transceiver unit; and

- an application controller unit coupled the protocol controller unit (MC in Fig 2) and coupled to the transceiver unit (Fig 2);

- wherein the transceiver unit causes the protocol controller unit to be supplied with voltage first, before the application controller unit is supplied with voltage (lines 45-65 of column 2 mention that activating demand on bus causes activating address filtering. Thus, address filter is supplied with voltage first. When intended address is received, the microcontroller is supplied with the voltage).

Heinrich does not teach that the transceiver and protocol controller are provided on different integrated circuits. Hanf et al teach a system where transceiver (100 in Fig 1) and protocol controller (22 in Fig 1; Fig 4) are provided on different integrated circuit.

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Heinrich and Hanf. One ordinary skill would be motivated to put the transceiver unit in different integrated circuit, as that would lead to a more flexible and modular design. Any commercially available transceiver chip may be used with the existing system.

For claim 26, Heinrich teaches that node can be maintained in low power mode when no data is transmitted via the bus line and interfaces are set to active state when activating demand is transmitted via the bus (line 50-60 of column 2). Fig 2 shows that IF takes power from line 15. Thus, when activating demand is in bus, protocol controller (i.e., part of interface) gets power from 15 to set into active state. Therefore, IF must comprise a first voltage controller that would determine when to supply the additional voltage for address filter (or, protocol controller). Hanf shows that the voltage regulator 110 is within integrated circuit.

Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Heinrich et al, in view of Hanf et al (US Patent 5892893), further in view of Hanf et al (US Patent 6438462).

For claim 27, UR in Heinrich is the voltage regulator to the application controller in the event of a match between an incoming message and a reference message. However, UR is not within the transceiver. Heinrich et al, in view of Hanf (US Patent 5892893) do not teach the two voltage regulators within one integrated circuit. Hanf et al (US Patent 6438462) teach two voltage regulators (Fig 14; lines 15-45 of column 35) in one circuit. One ordinary skill would be motivated to include two regulators in one circuit for better control of operation.

(10) Response to Argument

Appellant's arguments regarding claims 22-27 have been fully considered, but are not persuasive.

Regarding claim 22 and claim 25, appellant argues that the clock signal that is synchronized periodically to a clock master having a quartz oscillator is the clock signal MCclk (Heinrich Fig 6) provided to the microcontroller, not to the protocol controller, which is clocked by BITclk that is not synchronized to the clock master.

Examiner agrees that the clock signal that is synchronized periodically to a clock master having a quartz oscillator is the clock signal MCclk (Heinrich Fig 6) provided to the microcontroller (Fig 6, lines 20-25 of column 9). However, Examiner disagrees with the assertion that protocol controller is not provided with quartz oscillator input signal. In addition to microcontroller, part of the protocol controller "ASR" is also synchronized (i.e., provided) with the quart oscillator input signal (line 36, column 10 through line 5, column 11; Fig 4 – Fig 6 of Heinrich). Lines 36-44 of column 10 of Heinrich mention that the quartz oscillator determines the frequency and clock rate for the entire remainder of the data system. Lines 55-60 of column 10 of Heinrich mention that interfaces are addressed by the emission of a clock definition bit sequence of the clock master and a frequency synchronization takes place in all of the interfaces. Fig 6 shows that MCclk is derived from BITclk and Start. Fig 4 shows that BITclk and Start are generated from Rx,

the bit sequence received via bus 13. Fig 3 shows that BITclk is fed to ASR (lines 13-20 of column 6). As MCclk depends on BITclk, the quartz oscillator input is provided to both ASR and microcontroller. Therefore quart oscillator input is provided to protocol controller.

Regarding claim 23, appellant further argues that no handshaking between transceiver unit and the protocol controller occurs, since they are part of same circuit.

Examiner disagrees. Claim 23 requires the protocol controller unit ("ASR" and "AF" in Fig 3 in Heinrich) to be addressed by the incoming message (Rx; lines 38-55 of column 5), the transceiver unit conveying the incoming message to the protocol controller unit (Fig 3, Rx is fed to ASR, AF); the protocol controller unit comparing the incoming message with a reference message that is associated with the application and is stored in the protocol controller unit (lines 37-60 of column 5; lines 50-60 of column 2; lines 10-16 of column 3; the content of ASR is the incoming message, which is compared with the content of address filter. Address filter carries the address identification for the respective node. Such reference address is associated with the respective node, microcontroller and the applications of the microcontroller); if there is a match between the incoming message and the reference message (lines 21-32 of column 6), the protocol controller unit sending an acknowledgement to the transceiver unit (lines 33-38 of column 6 mention that acknowledgement Wint is sent to microcontroller. Therefore Wint is sent to transmitter, or part of transceiver when match exists); and the transceiver

unit, in response to the acknowledgement, activating the application controller unit (lines 60-65 of column 2; lines 42-46 of column 6). Therefore, Heinrich provides the necessary claimed limitations of claim 23.

Regarding claim 27, appellant argues that claim requires first and second voltage regulators for supplying the protocol controller and application controller units respectively, which is not taught by Hanf II, though Hanf II teaches two regulators.

Examiner disagrees. Claim 27 does not require first and second voltage regulators for supplying the protocol controller and application controller units respectively. Claim 27 requires a second voltage regulator for supplying voltage to the application controller. UR in Heinrich supplies voltage to application controller (Fig 2). Heinrich has another voltage regulator that regulates voltage to interface (lines 50-60 of column 2; Fig 2 shows that IF takes power from line 15 (lines 15-20 of column 1 mentions that voltage supply lines provide voltage to data nodes). Thus, when activating demand is in bus, protocol controller (i.e., part of interface) gets power from 15 to set into active state. Therefore, IF must comprise a first voltage controller/regulator that would determine when to supply the additional voltage for address filter, or protocol controller). Therefore UR can be considered as second voltage regulator. However, it is not clear whether they are within same integrated circuit. Hanf II teaches two regulators within same integrated circuit (lines 15-25 of column 35).

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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